

**REMARKS**

Claims 1-7, 9, 12-21, 24-25 and 27-30 are pending.

Claims 1-7, 9, 12-21, 24-25 and 27-30 are rejected.

In the office action dated May 28, 2008, claims 1-7, 9, 12-18 and 27-28 are rejected under 35 USC §103(a) as being unpatentable over a paper by Cantle ("A Foundation Architecture for Elevating DSP in FPGAS") in view of Dowling U.S. Patent No. 6,163,836 and Ferris US Publication No. 20030008684.

The '103 rejection has been rendered moot by the amendments above. New base claims 31 and 35 recite features for controlling the flow of data between an FPGA and a CPU during a numerical simulation. These features are not taught or suggested by the documents made of record.

Claim 17 has been amended to depend from new claim 32. In the rejection of claim 17, the office action cited pages 7-8 of Cantle. However, the relevance of pages 7-8 is not clear. If the rejection of claim 17 is maintained, the examiner is respectfully requested to explain how pages 7-8 support the '103 rejection of claim 17.

If the Examiner has any questions or wishes to further discuss this application, the Examiner is encouraged to contact the undersigned.

Respectfully submitted,

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